

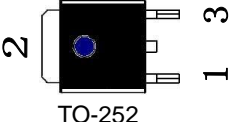

1、Description

Passivated, sensitive gate thyristors In a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low current power gate trigger circuits.

2、Features

- Blocking voltage to 600 V
- On-state RMS current to 12A
- Ultra low gate trigger current
- Low cost package.

3、Pinning information

PIN	Description	Simplified outline	Symbol
1	Cathode (K)		
2	Anode (A)		
3	Gate (G)		

4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	600	V
$I_{T(AV)}$	Average on-state current	7.6	A
$I_{T(RMS)}$	RMS on-state current	12	A
I_{TSM}	Non-repetitive peak on-state current	100	A

5、Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance	junction to case	-	-	2.2	°C /W
$R_{\theta JA}$		junction to ambient	-	-	88	°C /W
T_L	Maximum Lead Temperature for Soldering Purposes	1/8", from Case for 10 Seconds	-	-	260	°C

6、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages		-	600	V
$I_{T(AV)}$	Average on-state current	180°Conduction angles; $T_C=75^{\circ}\text{C}$	-	7.6	A
$I_{T(RMS)}$	RMS on-state current	180°Conduction angles; $T_C=75^{\circ}\text{C}$	-	12	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_J=110^{\circ}\text{C}$	-	100	A
I^2t	Circuit fusing Consideration	$t = 8.3 \text{ ms}$	-	41	A^2s
I_{GM}	Peak gate current	Pulse Width $\leq 1.0\mu\text{s}$, $T_C=75^{\circ}\text{C}$	-	2.0	A
P_{GM}	Forward Peak gate power	Pulse Width $\leq 1.0\mu\text{s}$, $T_C=75^{\circ}\text{C}$	-	5.0	W
$P_{G(AV)}$	Forward Average gate power	$T=8.3\text{msec}$, $T_C=75^{\circ}\text{C}$	-	0.5	W
T_{stg}	Storage temperature		-40	150	$^{\circ}\text{C}$
T_j	Operating junction temperature		-40	110	$^{\circ}\text{C}$

7、Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
V_{TM}	On-state voltage	$I_{TM} = 20\text{A}$	-	-	2.2	V
I_{GT}	Gate trigger current	$V_D = 12 \text{ V}$; $R_L = 100\Omega$; Continuous dc $T_J=25^{\circ}\text{C}$	2.0	4.0	15.0	mA
V_{GT}	Gate trigger voltage	$V_D = 12 \text{ V}$; $R_L=100\Omega$ $T_J=25^{\circ}\text{C}$	0.5	0.65	0.8	V
I_L	Latching current	$V_D = 12 \text{ V}$; $I_G = 2.0\text{mA}$; $T_J=25^{\circ}\text{C}$	6.0	12	30	mA
I_H	Holding current	$V_D = 12 \text{ V}$; Initiating Current=200mA; Gate Open; $T_J=25^{\circ}\text{C}$	4.0	10	20	mA
Dynamic Characteristics						
dv/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_J = 110^{\circ}\text{C}$; Exponential wave form; $R_{GK} = 1 \text{ k}\Omega$	100	250		$\text{V}/\mu\text{s}$
t_{gt}	Turn on time	Source Voltage=12V, $R_S=6.0\text{K}\Omega$, $I_T=16\text{A(pk)}$, $R_{GK}=1.0\text{K}\Omega$ $V_D=\text{Rated } V_{DRM}$, Rise Time=20ns. Pulse Width=10 μs	-	2.0	5.0	μs
di/dt	Critical Rate of Rise of On-State Current	$IPK = 50 \text{ A}$, $Pw = 40 \text{ sec}$, $diG/dt = 1 \text{ A/sec}$, $I_{gt} = 50 \text{ mA}$	-	-	50	A/s

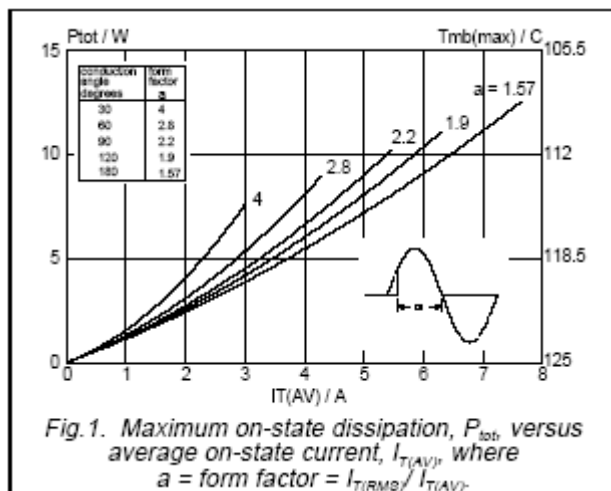


Fig. 1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$.

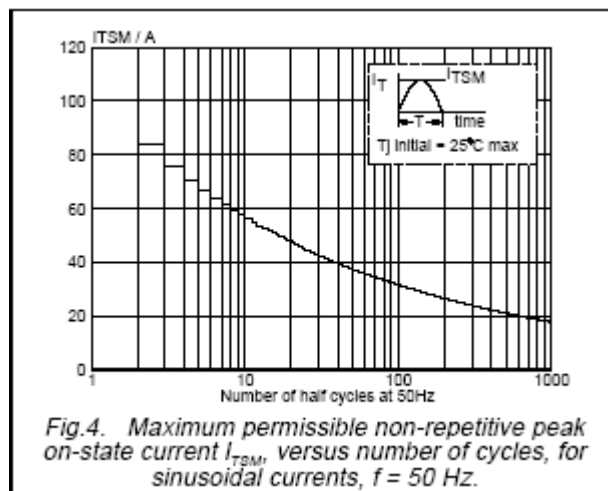


Fig. 4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 \text{ Hz}$.

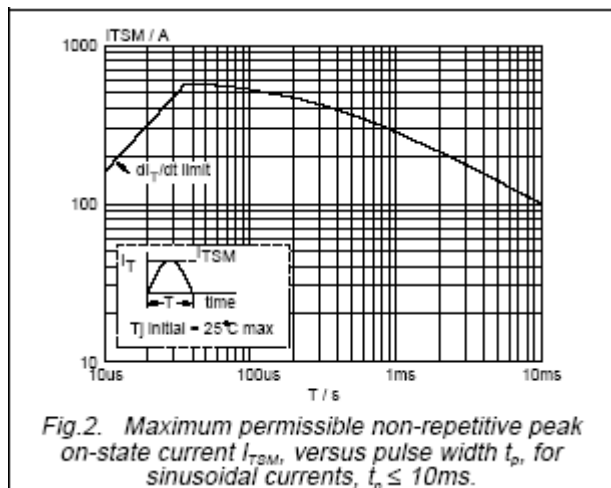


Fig. 2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10 \text{ ms}$.

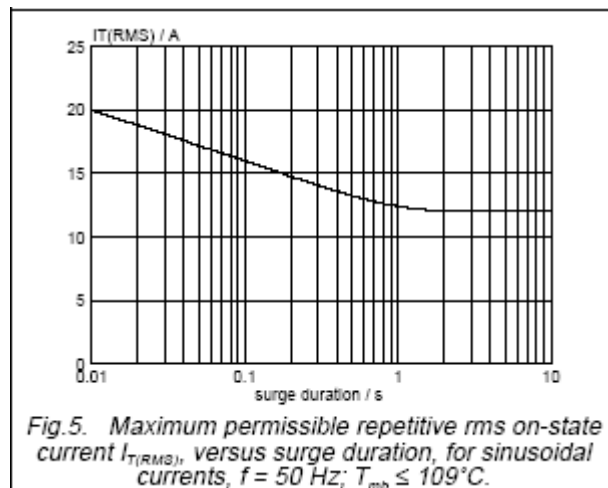


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 \text{ Hz}$; $T_{mb} \leq 109^\circ\text{C}$.

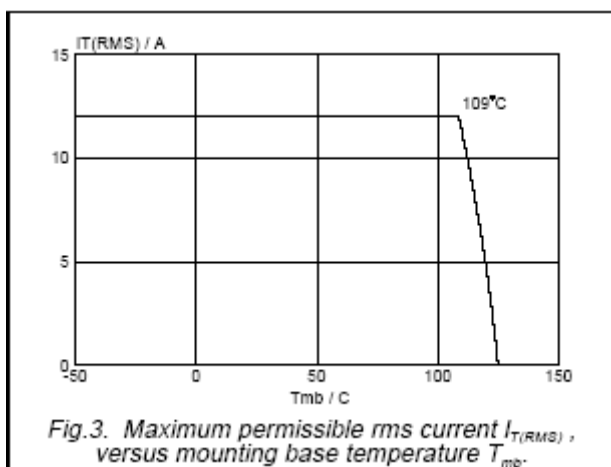


Fig. 3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb} .

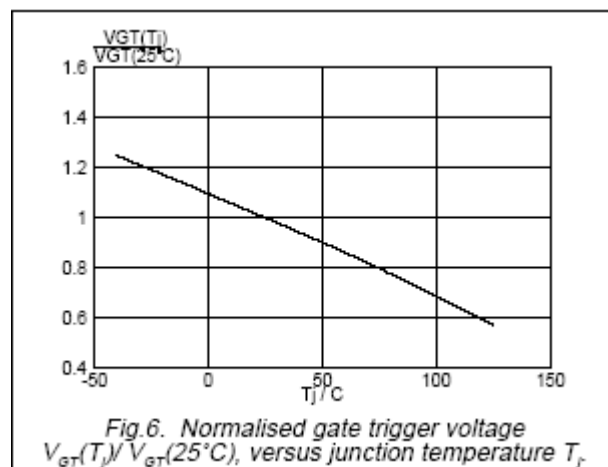
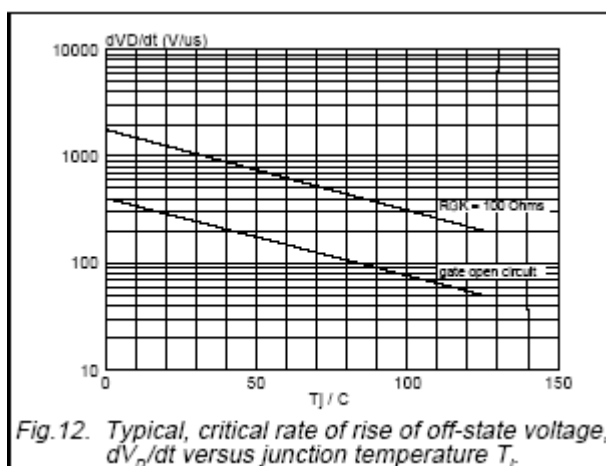
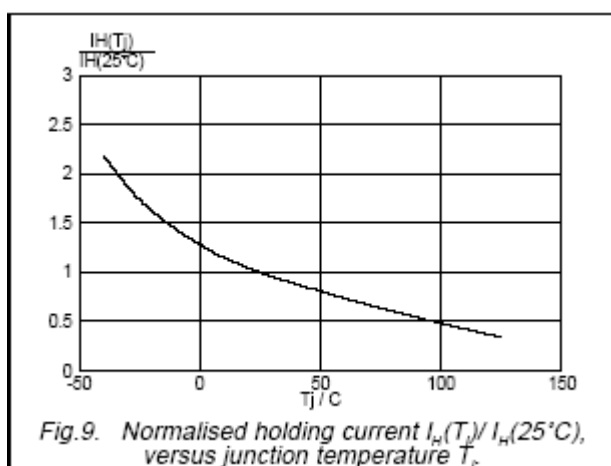
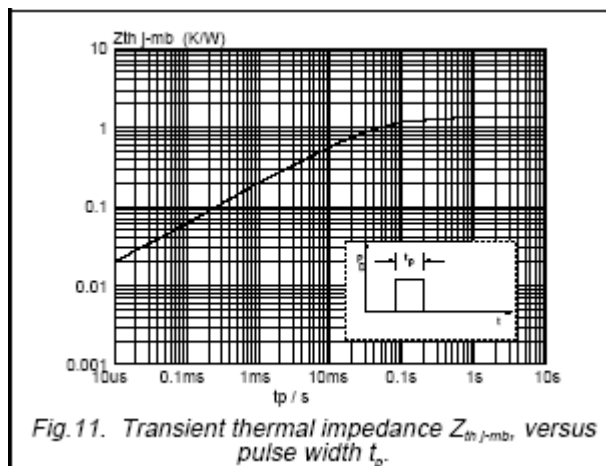
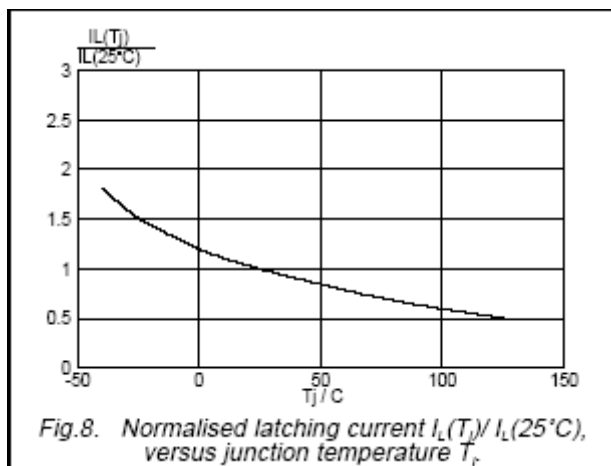
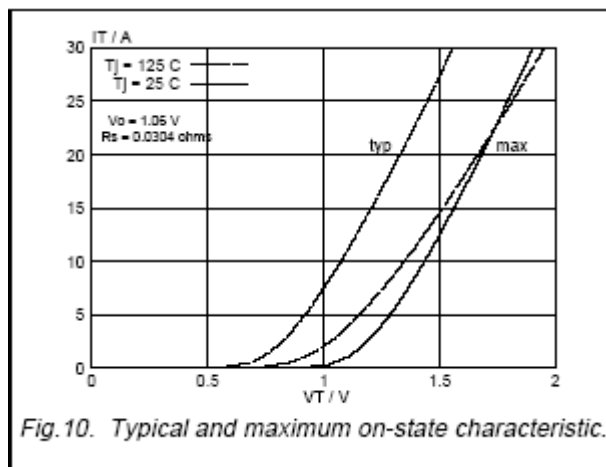
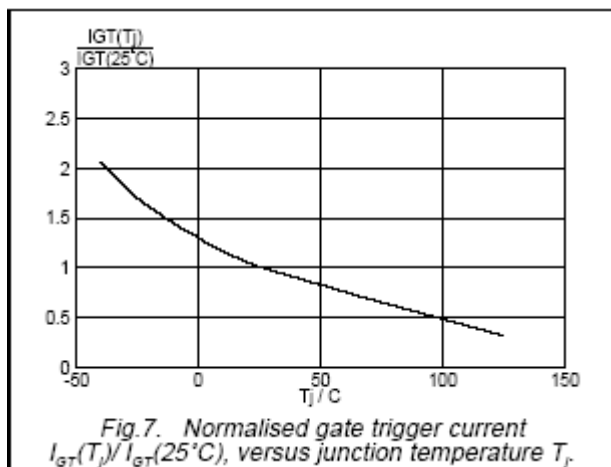
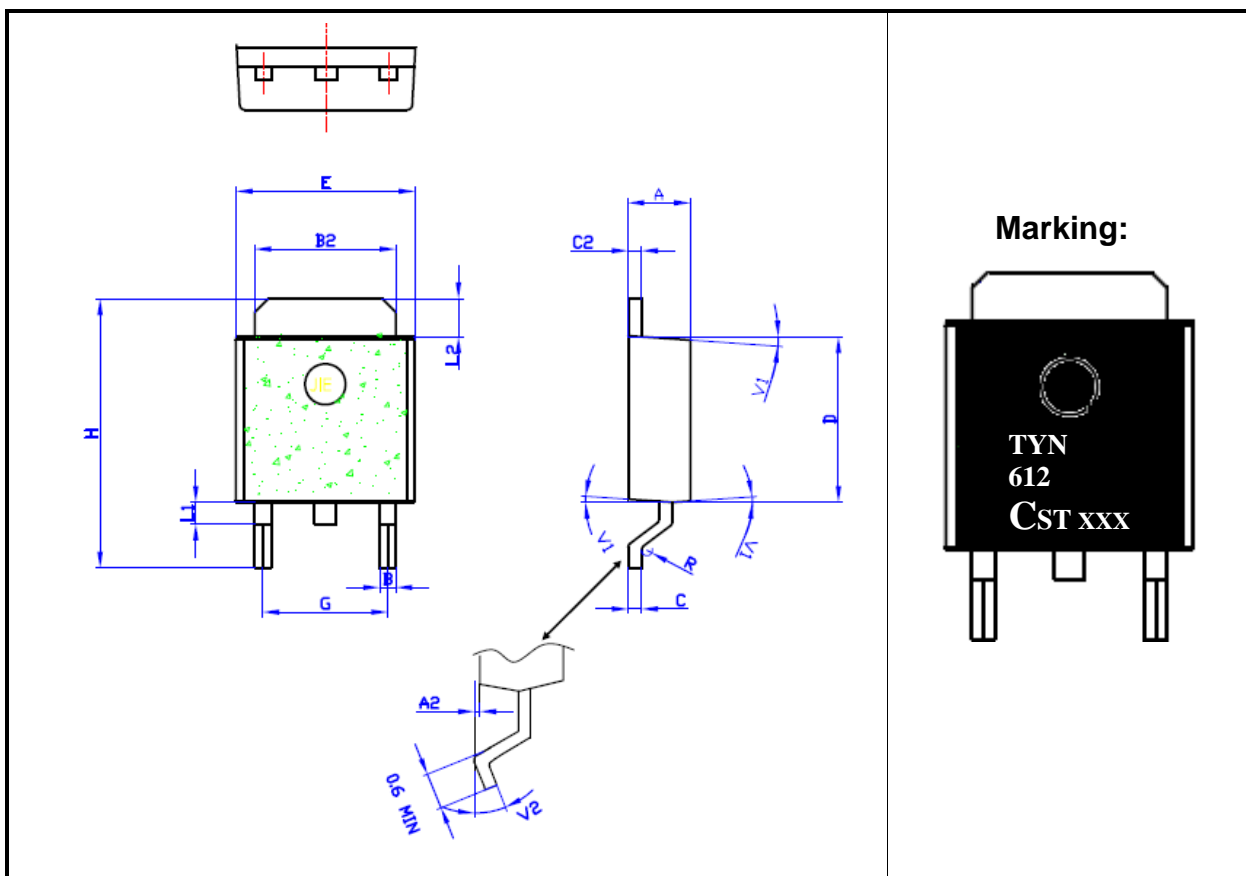


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .



9、Package outline(TO-252)



DIM	Inches			Millimeters		
	Min	Type	Max	Min	Type	Max
A	0.087	-	0.094	2.20	-	2.40
A2	0.001	-	0.009	0.03	-	0.23
B	0.022	-	0.026	0.55	-	0.65
B2	0.205	-	0.213	5.20	-	5.40
B3	0.030	-	0.033	0.76	-	0.85
B4	-	0.013	-	-	0.32	-
C	0.018	-	0.024	0.45	-	0.62
C2	0.016	-	0.021	0.40	-	0.54
D	0.236	-	0.244	6.00	-	6.20
E	0.252	-	0.260	6.40	-	6.60
G	0.173	-	0.181	4.40	-	4.60
H	0.384	-	0.419	9.75	-	10.65
L1	-	0.031	-	-	0.8	-
L2	0.071	-	0.075	1.80	-	1.90
V1	-	4°	-	-	4°	-
V2	0°	-	8°	0°	-	8°