Sensitive Gate SCRs BT151-800R

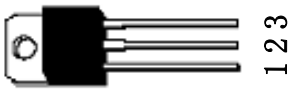
1、Description

Passivated, sensitive gate thyristors In a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low current power gate trigger circuits.

2、Features

- Blocking voltage to 800 V
- On-state RMS current to 12A
- Ultra low gate trigger current
- Low cost package.

3、Pinning information

PIN	Description	Simplified outline	Symbol
1	Cathode (K)	 TO-220	
2	Anode (A)		
3	Gate (G)		

4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	800	V
$I_{T(AV)}$	Average on-state current	7.6	A
$I_{T(RMS)}$	RMS on-state current	12	A
I_{TSM}	Non-repetitive peak on-state current	100	A

5、Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance	junction to case	-	-	2.2	°C /W
$R_{\theta JA}$		junction to ambient	-	-	88	°C /W
T_L	Maximum Lead Temperature for Soldering Purposes	1/8", from Case for 10 Seconds	-	-	260	°C

6、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages		-	800	V
$I_{T(AV)}$	Average on-state current	180°Conduction angles; T_C=75℃	-	7.6	A
$I_{T(RMS)}$	RMS on-state current	180°Conduction angles; T_C=75℃	-	12	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; T_J=110℃	-	100	A
I^2t	Circuit fusing Consideration	t = 8.3 ms	-	41	A^2s
I_{GM}	Peak gate current	Pulse Width≦1.0μs, T_C=75℃	-	2.0	A
P_{GM}	Forward Peak gate power	Pulse Width≦1.0μs, T_C=75℃	-	5.0	W
$P_{G(AV)}$	Forward Average gate power	T=8.3msec, T_C=75℃	-	0.5	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-40	110	°C

7、Characteristics

T_J = 25℃ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
V_{TM}	On-state voltage	I_{TM} = 20A	-	-	2.2	V
I_{GT}	Gate trigger current	V_D = 12 V; R_L = 100Ω; Continuous dc T_J=25℃	2.0	4.0	15.0	mA
V_{GT}	Gate trigger voltage	V_D = 12 V; R_L=100Ω T_J=25℃	0.5	0.65	0.8	V
I_L	Latching current	V_D = 12 V; I_G = 2.0mA; T_J=25℃	6.0	12	30	mA
I_H	Holding current	V_D = 12 V; Initiating Current=200mA; Gate Open; T_J=25℃	4.0	10	20	mA
Dynamic Characteristics						
dv/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 110 °C; Exponential wave form; R_{GK} = 1 kΩ	100	250		V/μs
t_{gt}	Turn on time	Source Voltage=12V, R_S=6.0KΩ, I_T=16A(pk),R_{GK}=1.0KΩ V_D=Rated V_{DRM}, Rise Time=20ns. Pulse Width=10μs	-	2.0	5.0	μs
di/dt	Critical Rate of Rise of On–State Current	IPK = 50 A, Pw = 40 sec, diG/dt = 1 A/ sec, Igt = 50 mA	-	-	50	A/ s

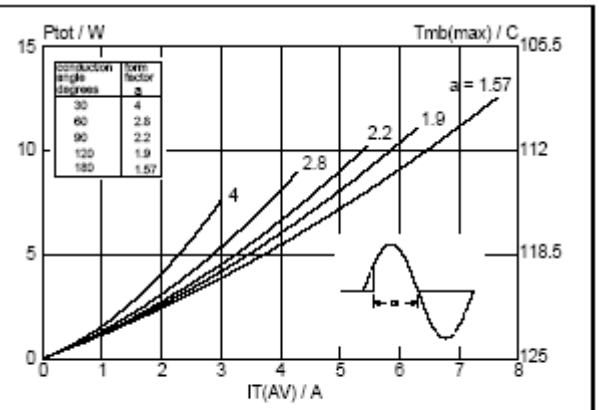


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}/ I_{T(AV)}$.

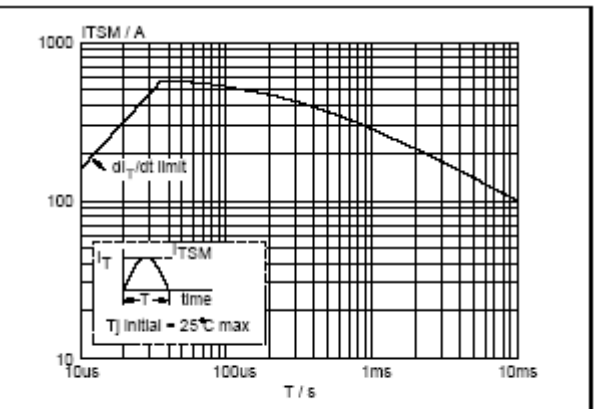


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 10ms$.

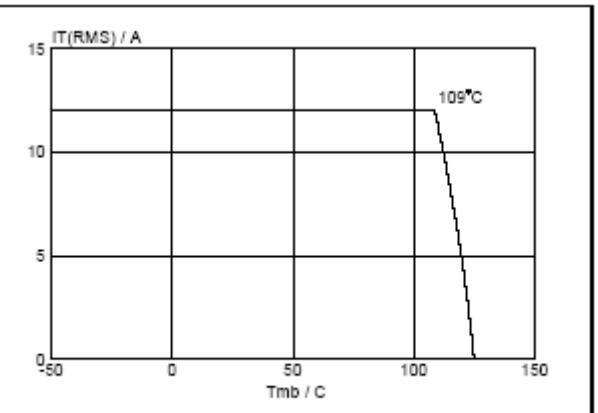


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

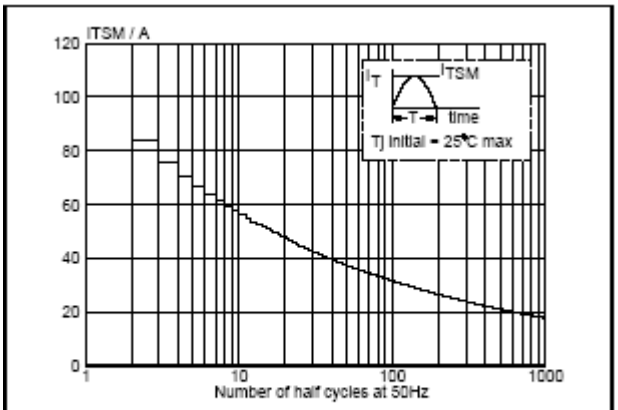


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

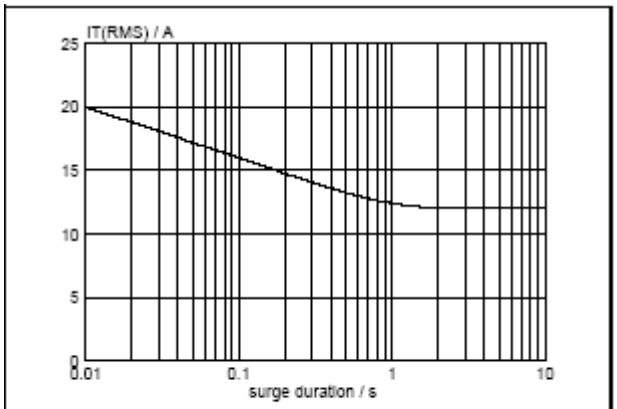


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 109°C$.

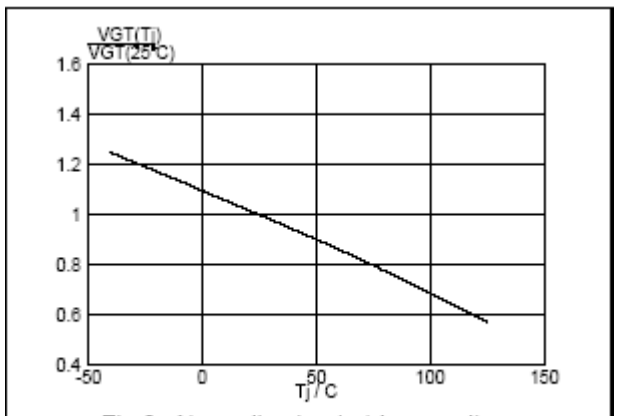


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

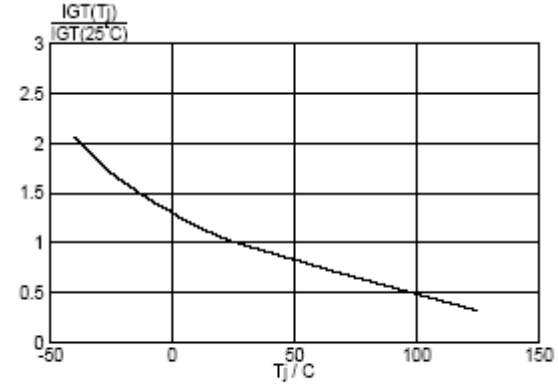


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

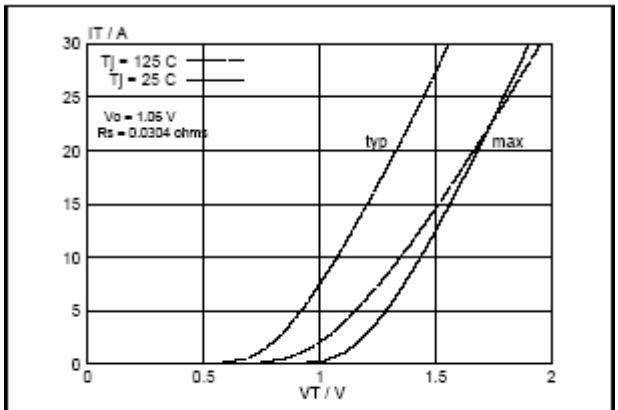


Fig.10. Typical and maximum on-state characteristic.

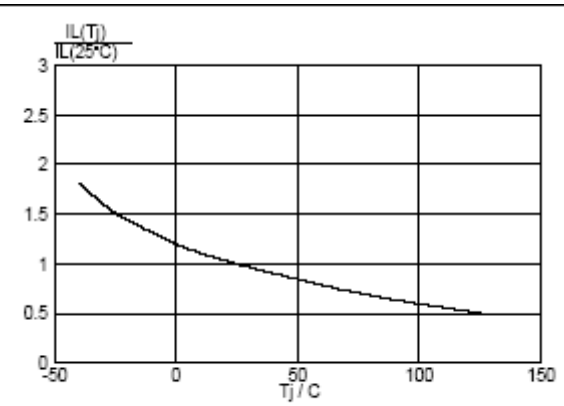


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

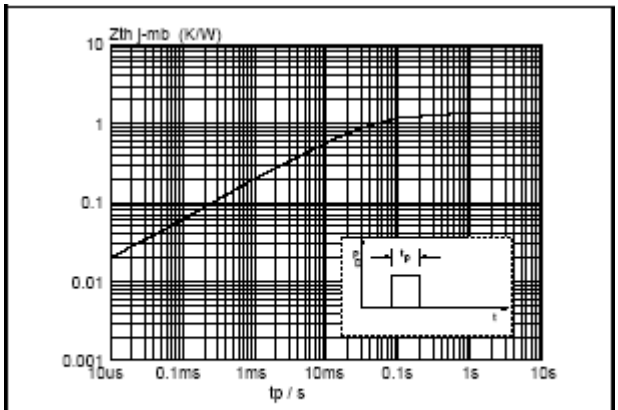


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

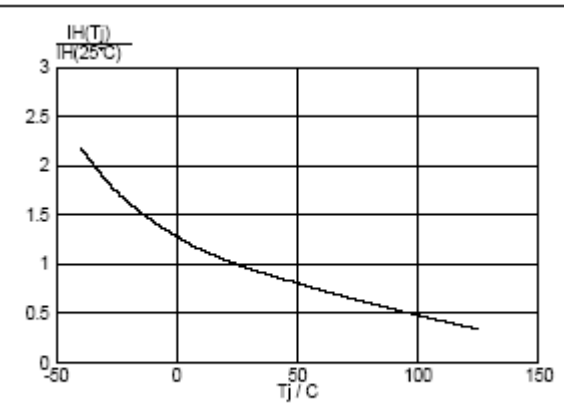


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

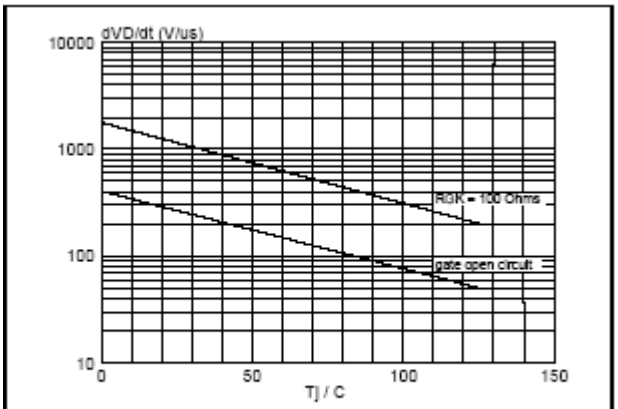
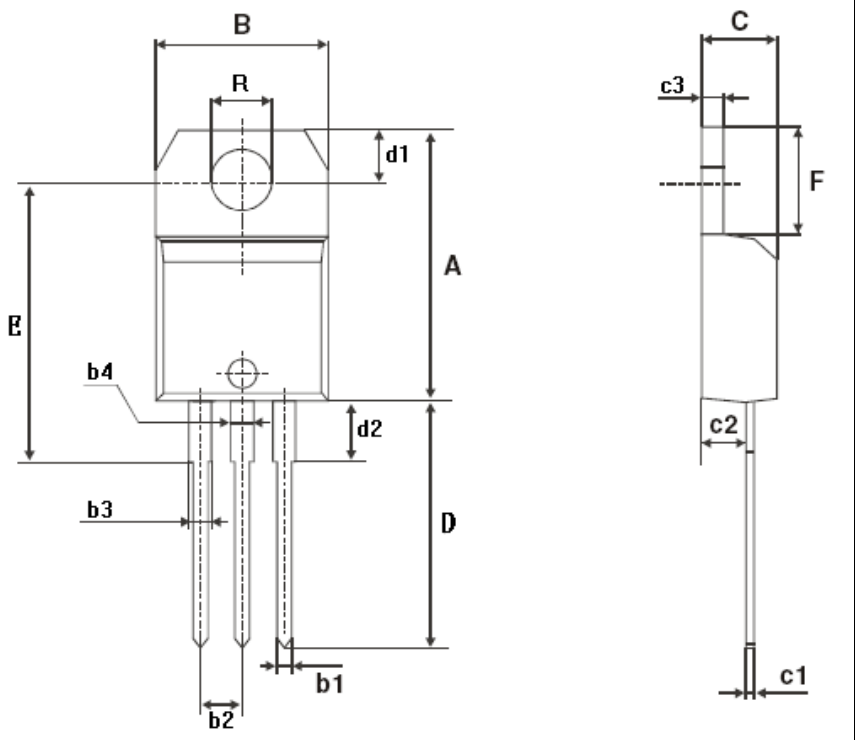
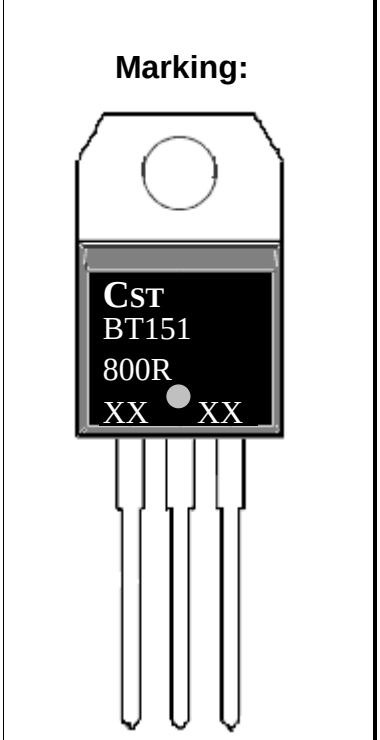


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

9、Package outline (TO-220I)





DIM	Inches			Milimeters		
	Min	Type	Max	Min	Type	Max
A	0.591	-	0.646	15.00	-	16.40
B	0.386	-	0.409	9.80	-	10.40
C	0.160	-	0.190	4.07	-	4.82
D	0.500	-	0.562	12.70	-	14.27
E	-	0.640	-	-	16.25	-
F	0.248	-	0.271	6.29	-	6.89
R	0.140	-	0.156	3.56	-	3.96
b1	0.030	-	0.037	0.75	-	0.95
b2	0.095	-	0.105	2.42	-	2.66
b3	0.046	-	0.054	1.17	-	1.37
b4	0.046	-	0.054	1.17	-	1.37
c1	0.017	-	0.023	0.42	-	0.58
c2	0.091	-	0.115	2.32	-	2.92
c3	0.045	-	0.055	1.15	-	1.39
d1	0.100	-	0.120	2.54	-	3.04
d2	0.125	-	0.155	3.18	-	3.93