TRIAC BT131

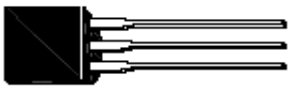
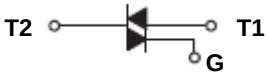
1、Description

Designed for use in solid state relays, MPU interface, TTL logic and any other light industrial or consumer application. Supplied in an inexpensive TO-92 package which is readily adaptable for use in automatic insertion equipment. Sensitive Gate Triggering In Four Trigger Modes for all possible Combinations of Trigger Sources, and Especially for Circuits that Source Gate Drives

2、Features

- Blocking voltage to 600V
- On-state RMS current to 1.0 A
- Sensitive Gate Triggering in Four Trigger Modes (Quadrants) for all possible Combinations of Trigger Sources, and especially for Circuits that Source Gate Drives
- All Diffused and Glassivated Junctions for Maximum Uniformity of Parameters and Reliability
- Low cost package.

3、Pinning information

PIN	Description	Simplified outline	Symbol
1	main terminal 1(T1)	 TO-92 1 2 3	 T2 T1 G
2	Gate(G)		
3	main terminal 2(T2)		
tab	main terminal		

4、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
$V_{DRM}V_{RRM}$	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	1.0	A
I_{TSM}	Non-repetitive peak on-state current	10	A

5、Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	*in free air*	-	-	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	*in free air*	-	-	200	°C/W
T_L	Maximum Lead Temperature for Soldering Purposes for 10 Seconds	*in free air*	-	-	260	°C

6、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DRM\&}V_{RRM}$	Repetitive peak off-state voltages		-	-	600	V
$I_{T(RMS)}$	RMS on-state current	Full Cycle Sine Wave 50 to 60 Hz (TC = +50 C)	-	-	1.0	A
I_{TSM}	Non-repetitive peak on-state current	One Full Cycle, Sine Wave 60 Hz (TC = 110 C)	-	-	10	A
I^2t	I^2t for fusing	t = 8.3 ms	-	-	0.26	A^2s
I_{GM}	Peak gate current		-	-	1.0	A
V_{GM}	Peak gate voltage		-	-	5.0	V
P_{GM}	Peak gate power		-	-	5.0	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	-	0.5	W
T_{stg}	Storage temperature		-40	-	150	°C
T_j	Operating junction temperature		-40	-	110	°C

7、Characteristics

T_J = 25℃ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	(V_D = 12 Vdc, R_L = 100 Ohms)				
		T2+ G+	-	3	5	mA
		T2+ G-	-	3	5	mA
		T2- G-	-	3	5	mA
		T2- G+	-	5	7	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1A				
		T2+ G+	-	1.6	10	mA
		T2+ G-	-	10.5	20	mA
		T2- G-	-	1.5	15	mA
		T2- G+	-	2.5	15	mA
I_H	Holding current	V_D = 12 V; Initiating Current = 200 mA, Gate Open	-	1.5	10	mA
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1A				
		T2+ G+	-	0.66	2.0	V
		T2+ G-	-	0.77	2.0	V
		T2- G-	-	0.84	2.0	V
		T2- G+	-	0.88	2.5	V
V_{GD}	Off-state leakage Voltage	V_D = 12 V, RL = 100 Ohms, T_J = 110 C ;All Four Quadrants	0.1	-	-	V
Dynamic Characteristics						
dv/dt(c)	Critical Rate–of–Rise of Commutation Voltage	V_D = Rated V_{DRM}, I_{TM} = .84 A, Commutating di/dt = .3 A/ms, Gate Unenergized, T_C = 50 C	-	5.0	-	V/μs
dv/dt	Critical Rate of Rise of Off–State Voltage	V_D = Rated V_{DRM}, T_C = 110 C, Gate Open, Exponential Waveform	-	25	-	V/μs
t_{gt}	Gate controlled turn-on time	V_D = Rated V_{DRM}, I_{TM} = 1.0 A pk, I_G = 25 mA	-	2.0	-	μs

8、Electrical Characteristics Curve

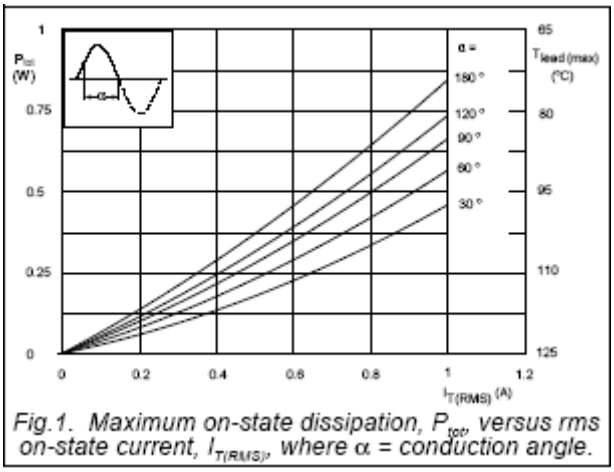


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

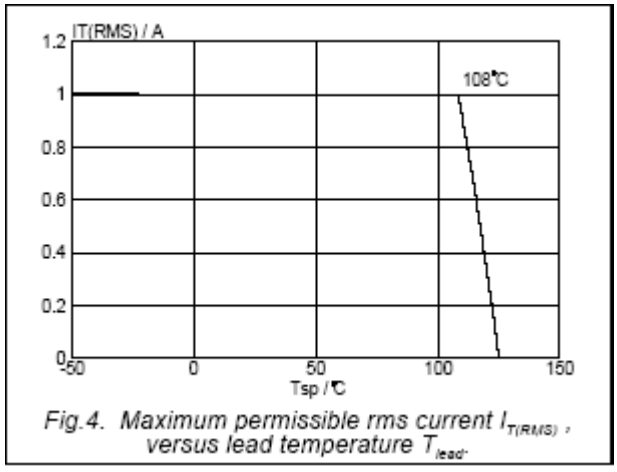


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead}.

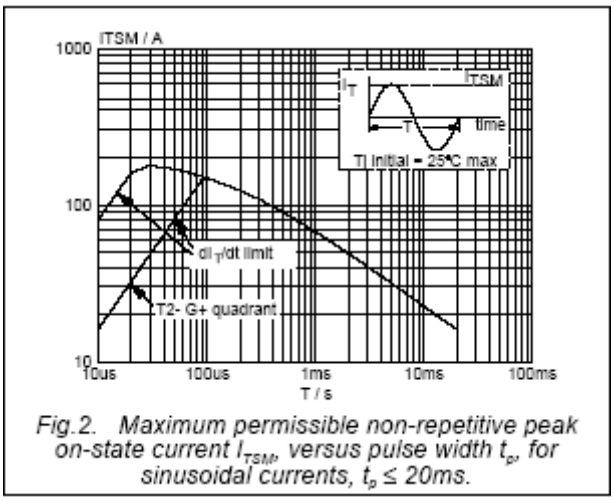


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

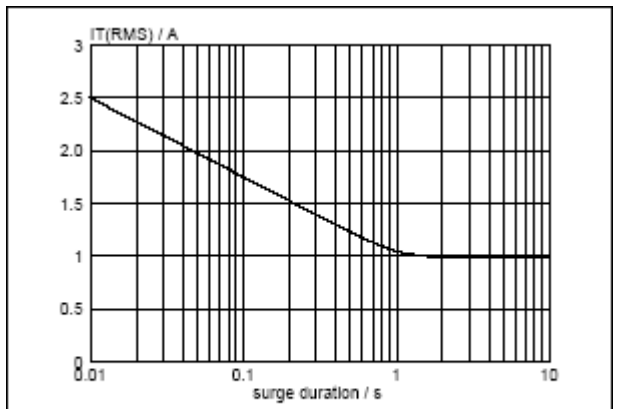


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 51°C$.

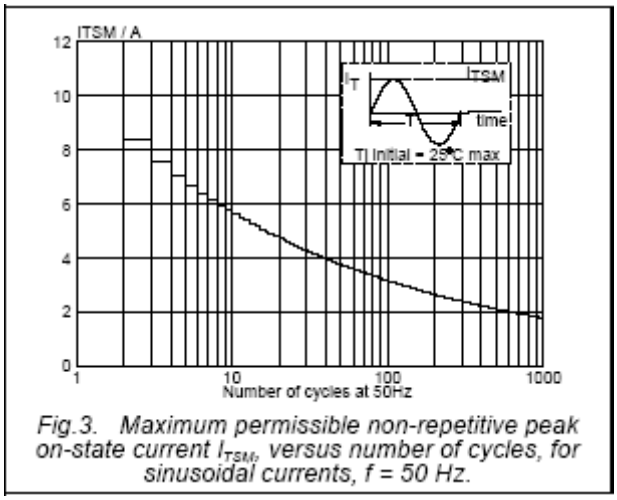


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

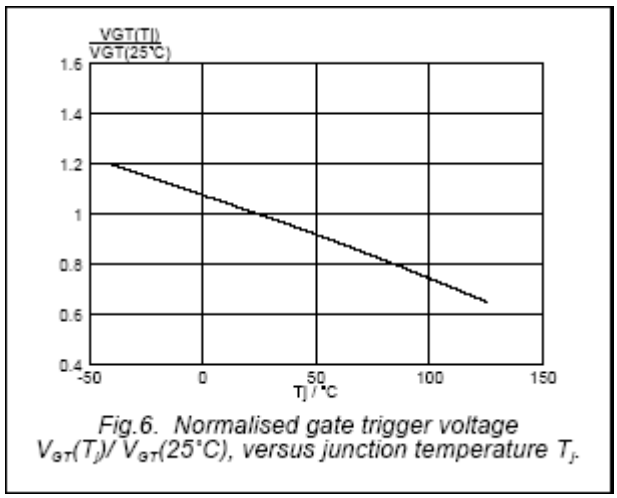


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

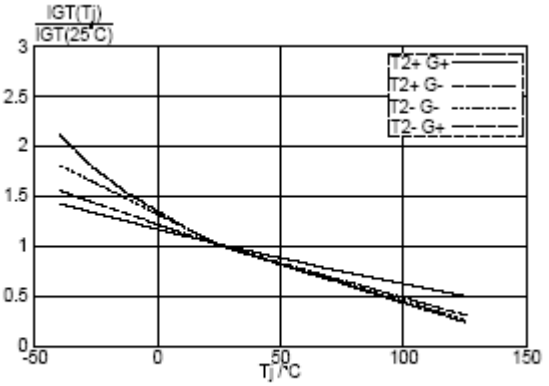


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

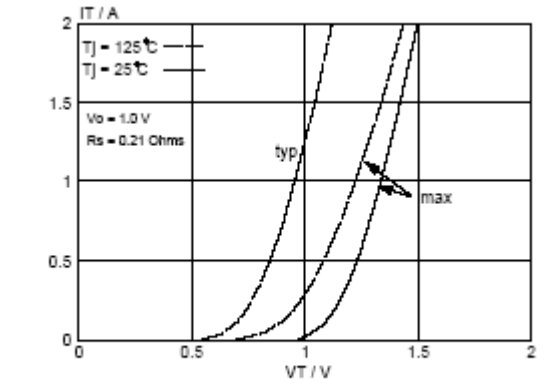


Fig.10. Typical and maximum on-state characteristic.

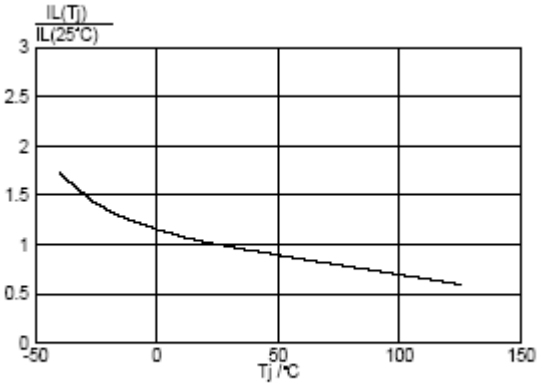


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

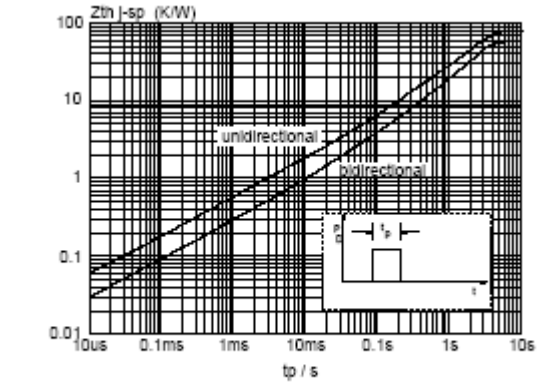


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}lead}$, versus pulse width t_p.

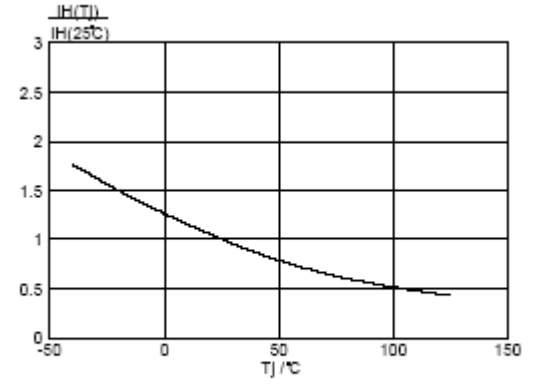


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

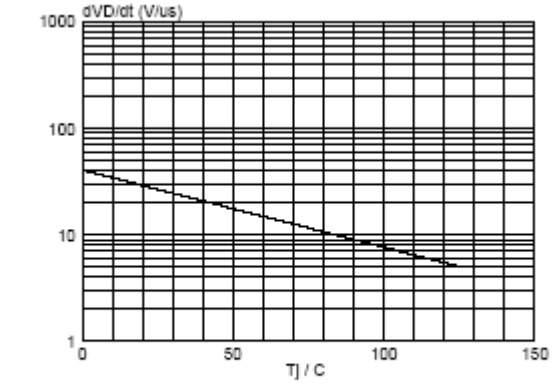
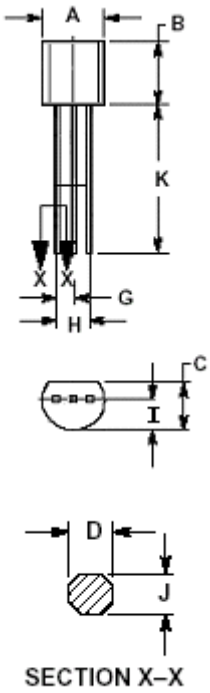
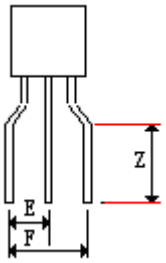


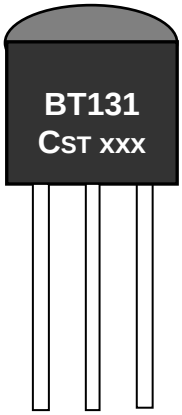
Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

9、Package outline(TO-92)





Marking:



DIM	Inches			Milimeters		
	Min	Type	Max	Min	Type	Max
A	0.175	-	0.205	4.45	-	5.20
B	0.170	-	0.210	4.32	-	5.33
C	0.134	-	0.142	3.40	-	3.60
K	0.500	-	-	12.70	-	-
G	0.045	-	0.055	1.14	-	1.39
H	0.095	-	0.105	2.41	-	2.67
I	0.080	-	0.105	2.04	-	2.66
D	0.016	-	0.021	0.41	-	0.53
J	0.012	-	0.018	0.30	-	0.45
E	0.08	-	0.112	2.15	-	2.85
F	0.179	-	0.215	4.55	-	5.45
Z	0.118	-	-	3.00	-	-