Four quadrant Triacs BT136 800E

1、Description

Passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting heating and static switching.

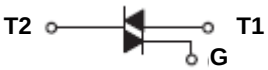
2、Applications

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

3、Features

- Blocking voltage to 800 V
- On-state RMS current to 4 A
- Ultra low gate trigger current
- Low cost package.

4、Pinning information

PIN	Description	Simplified outline	Symbol
1	main terminal 1(T1)	 TO-220	
2	main terminal 2(T2)		
3	gate (G)		
tab	main terminal 2		

5、Quick reference data

SYMBOL	PARAMETER	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	800	V
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	30	A

6、Thermal characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	*in free air*	-	-	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	*in free air*	-	-	75	°C/W
T_L	Maximum Lead Temperature for Soldering Purposes for 10 Seconds	*in free air*	-	-	260	°C

7、Limiting value

Limiting values in accordance with the Maximum System(IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages		-	800	V
$I_{T(RMS)}$	RMS on-state current	Full Cycle Sine Wave 50 to 60 Hz (TC = 85°C)	-	4	A
I_{TSM}	Non-repetitive peak Surge current	One Full cycle, 60 Hz, T_J = +110°C	-	30	A
I^2t	I^2t for fusing	t =8.3ms	-	3.7	A^2s
V_{GM}	Peak gate voltage	Pulse Width ≤ 1.0 μs, TC = 85°C	-	5	V
P_{GM}	Peak gate power	Pulse Width ≤1.0 μs, TC = 85°C	-	10	W
$P_{G(AV)}$	Average gate power	Pulse Width ≤1.0 μs, TC = 85°C	-	0.5	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-40	110	°C

8、Characteristics

T_J = 25℃ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1A T2+ G+ T2+ G- T2- G- T2- G+	 - - - -	 3 3 3 5	 10 10 10 25	 mA mA mA mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1A T2+ G+ T2+ G- T2- G- T2- G+	 - - - -	 1.5 5 1.0 3.0	 15 20 15 20	 mA mA mA mA
I_H	Holding current	Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current ≤1 Adc T_J = 25°C T_J =-40°C	 - -	 - -	 15 30	mA
V_{TM}	On-state voltage	I_{TM} = ±6 A Peak	-	1.4	2	V
V_{GT}	Gate trigger voltage (Continuous dc)	Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = –40°C All Quadrants	-	1.4	2.5	V
V_{GD}	Gate Non–Trigger Voltage	Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = 110°C All Quadrants	0.2	-	-	V
Dynamic Characteristics						
dV/dt(c)	Critical rate of rise of off-state voltage	V_{DRM}, TJ = 85°C, Gate Open, I_{TM} = 5.7 A, Exponential Waveform, Commutating di/dt = 2.0 A/ms	-	5	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM} = 14 Adc, I_{GT} = 100 mAdc	-	1.5	-	μs

9、Electrical Characteristics Curve

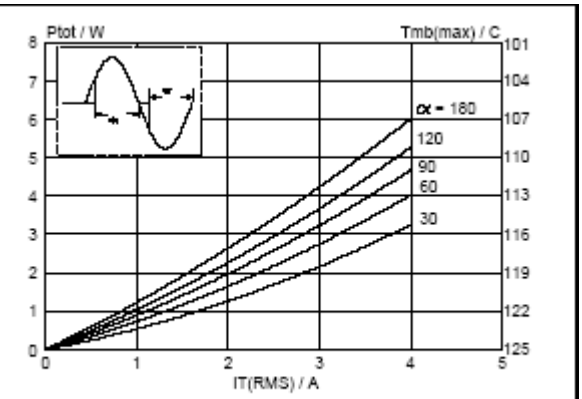


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

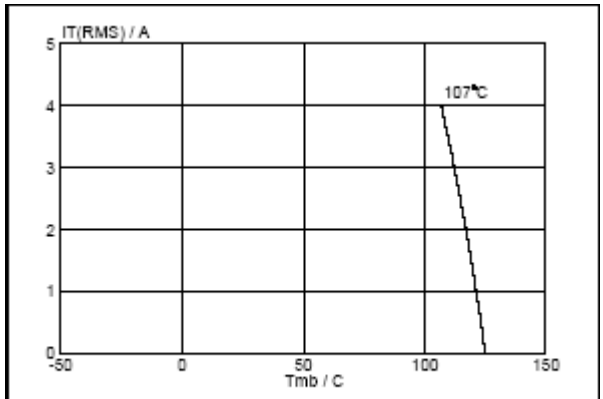


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

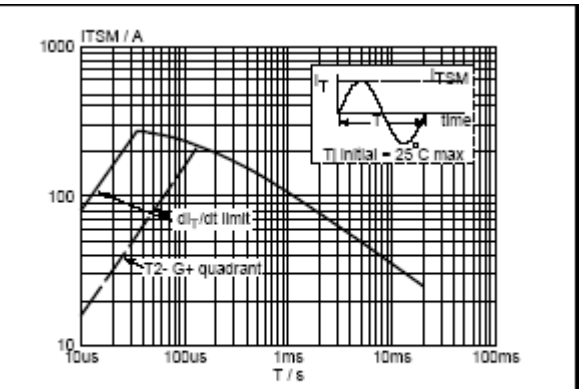


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

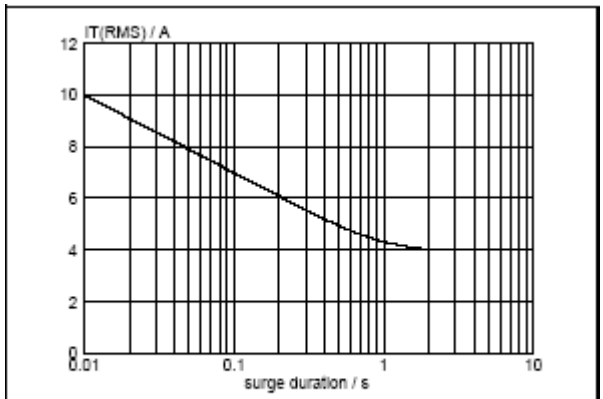


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.

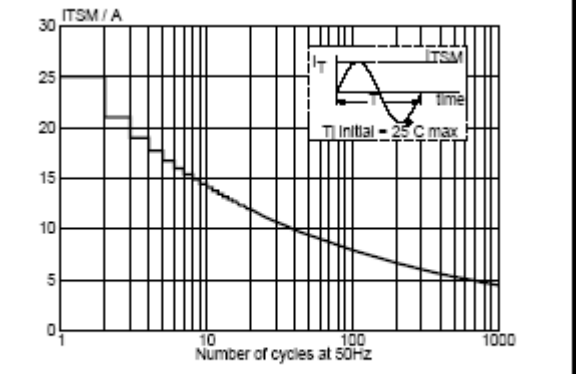


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

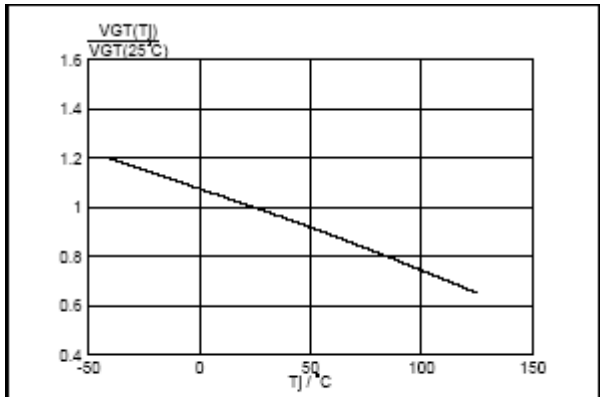


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

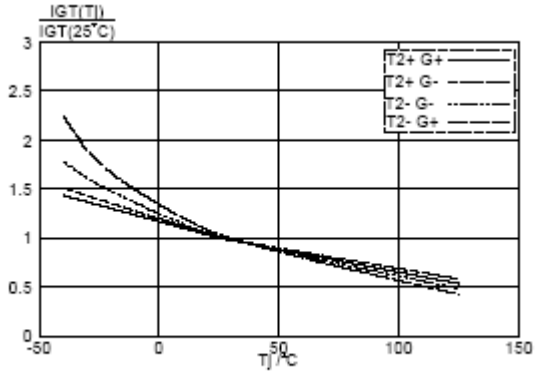


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

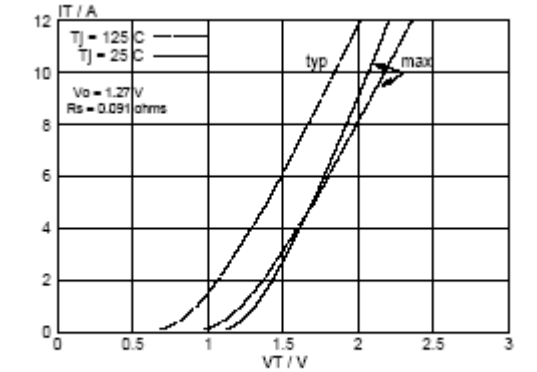


Fig.10. Typical and maximum on-state characteristic.

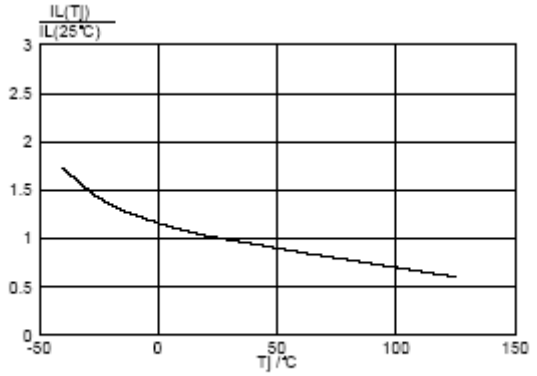


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

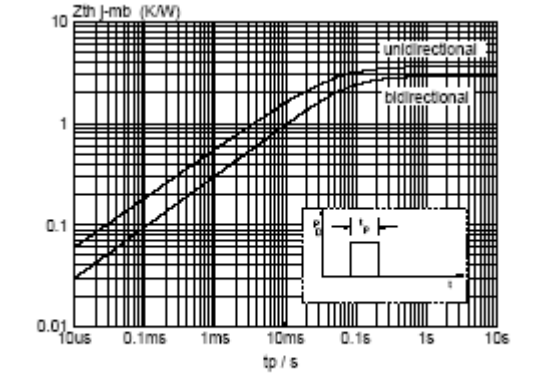


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

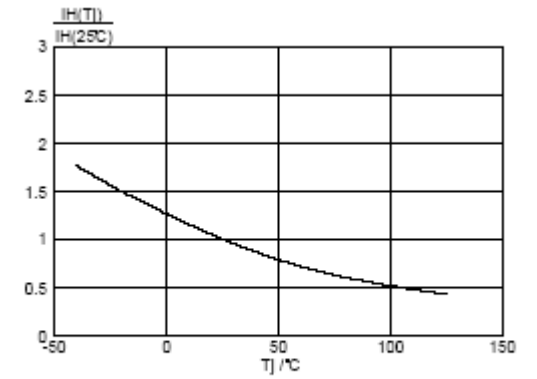


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

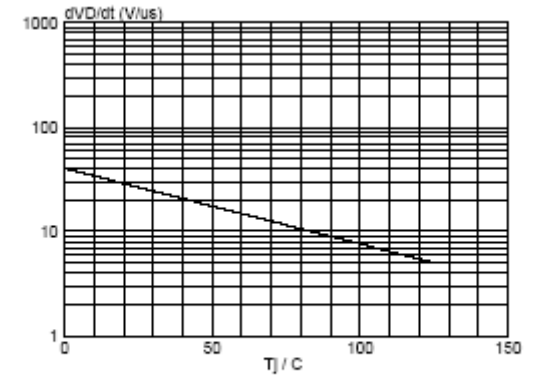
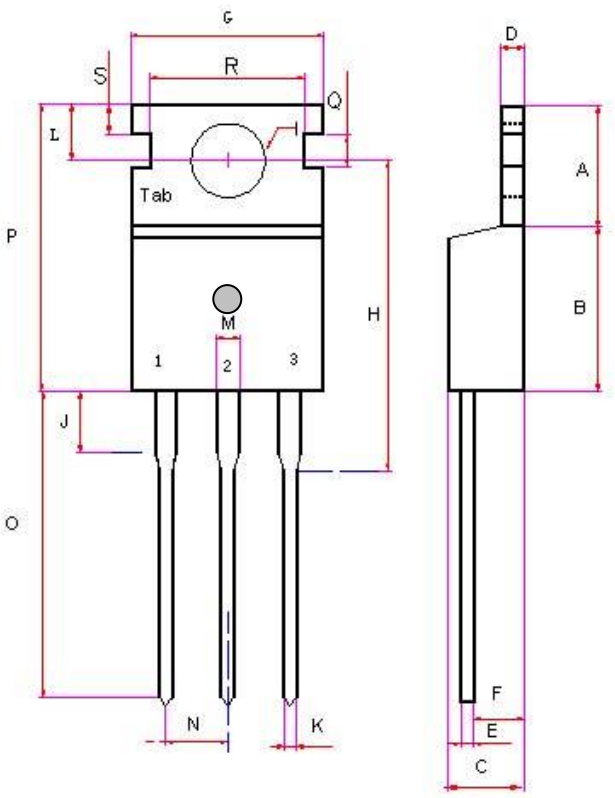
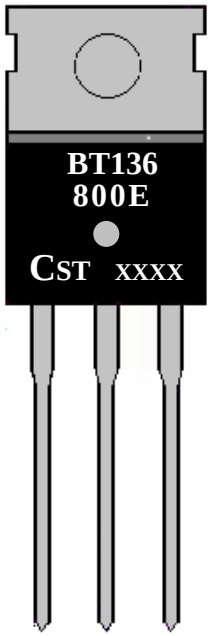


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

10、Package outline(TO-220)



Marking:



DIM	Inches			Milimeters		
	Min	Type	Max	Min	Type	Max
A	0.226	0.258	0.301	5.75	6.55	7.65
B	0.349	0.362	0.369	8.86	9.20	9.38
C	0.171	0.178	0.183	4.35	4.53	4.65
D	0.046	0.051	0.055	1.16	1.30	1.40
E	0.018	0.020	0.026	0.45	0.51	0.65
F	0.070	0.094	0.105	1.785	2.40	2.675
G	0.367	0.394	0.415	9.31	10.00	10.55
H	-	-	0.640	-	-	16.25
I	-	0.143	0.152	-	3.62	3.85
J	0.087	0.108	0.127	2.22	2.75	3.22
K	0.027	0.031	0.035	0.68	0.8	0.88
L	0.093	-	0.128	2.36	-	3.24
M	0.046	0.048	0.057	1.18	1.22	1.44
N	-	0.100	0.104	-	2.54	2.65
O	0.485	0.514	0.546	12.32	13.05	13.88
P	0.593	0.616	0.648	15.07	15.65	16.47
Q	0.057	0.067	0.073	1.46	1.7	1.86
R	0.320	0.344	0.360	8.14	8.75	9.14
S	0.046	0.051	0.058	1.17	1.3	1.47